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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/770,699	01/26/2001	F. Daniel Gealy	98093DIV	7854

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KIRKPATRICK & LOCKHART LLP
535 SMITHFIELD STREET
PITTSBURGH, PA 15222

EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,699	GEALY ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-43,45-49 and 52-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-43,45-49 and 52-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030822*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment and RCE filed on February 17, 2004. Claims 38-43,45-49,52-60 are currently pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim rejections - 35 USC § 103

1. Claims 38-39,42-43,45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al (6,165,834) taken with Prall et al (5,866,453).

Agarwal et al teach a method for forming a capacitor comprising at least the steps of: forming a first electrode (38 in Fig 5; col 5, lines 14-30; 24 in Fig 2; col 3, lines 42-45) selected from a group consisting of a conductive metal oxide; forming a dielectric (40 in Fig 5, col 5, lines 14-30; 26 in Fig 2; col 3, lines 55-65) on the first electrode, wherein the first electrode 38 is in a recess of a substrate assembly including the interlayer insulating layer having the shared bit contact 46 in the recess, the wordline 48, and the spacers adjacent to the wordline 48, and extends above an uppermost surface of a substrate assembly including the insulating layer for forming the recess, the wordline 48, and the spacers adjacent to the wordline 48, and an interconnect recessed in the substrate assembly; and forming a second electrode having a strap (42 in Fig 5; 30,38 in Fig 2; col 4, line 62 through col 5, line 7) on the dielectric and the uppermost surface of the substrate assembly including a layer 48, an interlayer insulating layer having bit contact 46, and an interconnect recessed in the substrate assembly, wherein the dielectric is formed between the first and second electrodes, wherein the metal oxide includes CVD Ruthenium dioxide, RuO_2, wherein x = 2, wherein the second capacitor electrode includes Platinum, TiN, Ru, WN, polysilicon, and wherein the dielectric 40,26 includes barium strontium titanate (BST), $SrTiO_3$, (Ba, $Sr_)TiO_3$, Ta_2O_5 (col 3, lines 55-65).

In Agarwal, Figure 5, the first electrode 38 is not extended above the substrate assembly including the interlayer insulating layer having the bit contact 46 (Fig 5).

However, Prall teaches two alternative embodiments, wherein as shown in Figure 7, a first electrode 42 extends above the substrate assembly including the interlayer insulating film 36 so as to expose more surfaces of the capacitor electrode 42 (Figs 4,7), and wherein, in a second

embodiment as shown in figure 17, the first electrode 42 is recessed and not extended above the substrate assembly including the interlayer insulating layer 45.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor of Agarwal by alternatively forming the first electrode extends above the substrate assembly as taught by Prall. This is because of the desirability to expose more surface of the capacitor electrode so as to increase capacitance of the capacitor, and thus, form a capacitor structure having higher capacitance, wherein the first electrode of the capacitor extending above the substrate assembly is formed by removing the insulating walls around the outer periphery of the storage node first electrode.

2. Claims 40,41-43,45,48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al (6,165,834) and Prall et al (5,866,453), as applied to claims 38-39,42-43,45-49 above, and further of Fukuzumi et al (6,222,722).

The references including Agarwal and Prall teach a method for forming a capacitor as applied to claims 38-39,42-43,45-49 above.

The references including Agarwal and Prall disclose many alternative materials for the electrodes or dielectric, but does not list all materials as recited in claims 40,41-43,45,48.

However, Fukuzumi et al teach a method for forming a capacitor, wherein the first electrode 13,52 of metal includes ruthenium, platinum, Ir, Rh, and its metal oxide including RuO_2, wherein x = 2 (col 14, line 66 through col 15, line 10; col 9, lines 49-67; col 16, line 62 through col 7; col 20, lines 10-25), wherein the second electrode 15,54 includes ruthenium, platinum, wherein materials for forming the electrode includes ruthenium, platinum, oxide thereof, or W, WN, Al, Ti, TaN (col 17, lines 12-18), wherein the dielectric 14,53 includes barium strontium titanate (BST), Ta_2O_5, $SrTiO_3$, $BaSrTiO_3$ (col; 17, lines 3-10).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electrodes or the dielectric of Agarwal by employing other alternative materials as known in the semiconductor art, as taught by Fukuzumi and Agarwal. This is because the substitution of art recognized equivalent materials would have been obvious and within the level of ordinary skill in the semiconductor art, wherein these dielectric materials

are having high dielectric constant, and wherein these conductive materials are oxidation barrier and having high electrical conductivity. Re further claim 40, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor electrode of Agarwal in the opening by planarization after CVD forming the first electrode as taught by Fukuzumi (Fig 4; col 7, lines 40-59), because of the desirability to isolate a plurality of lower electrodes one from each other, and to form stacked container capacitor having high capacitance.

3. Claims 38-43,45-49,52-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzumi et al (6,222,722) taken with Agarwal et al (6,165,834) and Chen et al (6,077,742).

Fukuzumi et al teaches a method for forming a capacitor comprising at least the steps of: forming on a substrate assembly a layer of hemispherical grain polysilicon (12 in Fig 11; col 9, line 45 through col 10; 51 in Figs 30-34; col 14, line 45 through col 15) in a recess of a substrate assembly including the layer (10 in Fig 11; 21/20 in Figs 22,27-29) and the layer (2 in Figs 11,22; 20/38 in Figs 27-29), wherein a portion of the substrate assembly is removed; forming a planarization first electrode of a CVD metal (13 in Fig 12; col 7, lines 40-60; or 52 in Figs 30-34) on the polysilicon, wherein the first electrode is selected from a group consisting of transition metal or a conductive metal oxide; forming a dielectric 14,53 on the first electrode, wherein the first electrode extends above an uppermost surface of a substrate assembly including the insulating interlayer (20 in Figs 27-29; or 66/10 in Fig 38), the insulating layer 2 and an interconnect 3 recessed in the assembly (Figs 6,24,26,27-29,38); and forming a second electrode having strap (15 in Fig 13; 54 in Fig 33) on the dielectric, wherein the dielectric is formed between the first and second electrodes, wherein the first electrode 13,52 of metal including ruthenium, platinum, Ir, Rh and its metal oxide including RuO_2, wherein x = 2 (col 14, line 66 through col 15, line 10; col 9, lines 49-67; col 16, line 62 through col 7; col 20, lines 10-25), wherein the second electrode 15,54 including ruthenium, platinum, wherein material for forming the electrode including ruthenium, platinum, oxide thereof, or W, WN, Al, Ti, TaN (col 17, lines 12-18), wherein the dielectric 14,53 includes barium strontium titanate (BSTO), Ta_2O_5, $SrTiO_3$, $BaSrTiO_3$ (col; 17, lines 3-10), wherein removing the hemispherical grain polysilicon 23,4 is shown in Figs 22-23, 4-5, wherein the substrate assembly comprising an interconnect 3 recessed

in the substrate (Figs 1-5,21-24,33,38), wherein the substrate assembly comprises a contact (Figs 21-24,333,38), and wherein the first electrode formed in the contact and the interconnect recessed in the substrate.

Fukuzumi already teaches to form the dielectric 8 on the first electrode 7 and on the uppermost surface of the substrate assembly 2, but lacks to form the second electrode 9 (or 15,27) on the substrate assembly.

However, Agarwal teaches (a first embodiment at Figures 3-4) forming a first planar capacitor having the second electrode 30/28 formed on the dielectric 26 formed on the first electrode 24 and the uppermost surface of the substrate assembly 16. Agarwal then teaches (a second embodiment at Figure 5) forming a second capacitor in trench by forming the capacitor dielectric 40 at the selected portion of the substrate, on the first electrode 38, and on an uppermost surface of the substrate assembly, and forming the second electrode 42 on the dielectric 40 and the uppermost surface of the substrate assembly. Chen teaches (at Figs 5-8; col 8, line 35 through col 9) forming a first electrode 36' in a recess of a substrate assembly and extending above the uppermost surface of the substrate assembly including an insulating layer 32/28 (Fig 5); forming a capacitor dielectric 40 on the first electrode 36' and the uppermost surface of the substrate assembly including the insulating layer 32/28; and forming the second electrode 42 on the dielectric 40 and the uppermost surface of the substrate assembly including the insulating layer 32/28.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor of Fukuzumi by forming the capacitor dielectric layer on the first electrode, and forming the second electrode entirely on the capacitor dielectric layer and on the uppermost surface of the substrate assembly, as disclosed by Agarwal and Chen. This is because of the desirability to form a trench capacitor having a planar electrode structure, as shown in Figure 5 of Agarwal, wherein there is no high step formed due to patterning both of the second electrode and the dielectric layer. This is also because of the desirability to form the top second electrode to entirely cover the capacitor dielectric layer. This is also because of the desirability to complete and facilitate the next level of electrical interconnections in forming an electrical contact to the second electrode 42 that is laterally extended from the first electrode,

and formed on the uppermost surface of the substrate assembly including the insulating layer 32/28 (Chen, Fig 8; col 9, lines 55 through col 10, line 4).

Re further claims 41-43,45,58, Fukuzumi teaches many alternative materials for forming the electrodes or dielectric, but does not list all materials. Indeed, Fukuzumi teaches a method for forming a capacitor as applied above to claims 38-43,45-49,52-57, wherein the first electrode 13,52 of metal includes ruthenium, platinum, Ir, Rh, and its metal oxide including RuO_2, wherein x = 2 (col 14, line 66 through col 15, line 10; col 9, lines 49-67; col 16, line 62 through col 7; col 20, lines 10-25), wherein the second electrode 15,54 includes ruthenium, platinum, wherein materials for forming the electrode include ruthenium, platinum, oxide thereof, or W, WN, Al, Ti, TaN (col 17, lines 12-18), wherein the dielectric 14,53 includes barium strontium titanate (BST), Ta_2O_5, $SrTiO_3$, $BaSrTiO_3$ (col; 17, lines 3-10). Agarwal also teaches forming the dielectric between the first and second electrodes, wherein the metal oxide includes CVD Ruthenium dioxide, RuO_2, wherein x = 2, wherein the second capacitor electrode includes Platinum, TiN, Ru, WN, IrO, RuO, Pt, Ir, polysilicon (col 3, lines 42-45; col 5, lines 1-7), wherein the dielectric 40,26 includes barium strontium titanate (BST), $SrTiO_3$, (Ba, $Sr_)TiO_3$, Ta_2O_5 (col 3, lines 55-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electrodes or the dielectric of Fukuzumi by using other alternative materials as well known in the semiconductor art and as combinatively taught by Fukuzumi and Agarwal. This is because the substitution of art recognized equivalent materials would have been obvious and within the level of ordinary skill in the semiconductor art, wherein these dielectric materials are having high dielectric constant, and wherein these conductive materials are oxidation barrier and having high electrical conductivity. Re further claim 40, planarization after CVD forming the first electrode is taught by Fukuzumi (at Fig 4; col 7, lines 40-59), because of the desirability to isolate a plurality of lower electrodes one from each other, and to form stacked container capacitor having high capacitance.

Response to Amendment

*** Regarding 35 USC 102 rejection using Agarwal (6,165,834): Applicant's convincing remarks filed February 17, 2004 have overcome the rejection in the last office action, wherein

the first electrode 38 is formed in a recess formed in an interlayer insulating layer having the shared bit contact 46, but not extended above the uppermost surface of the substrate assembly having the interlayer insulating layer having the shared bit contact 46.

*** Rejection using Fazan (5,478,772) as a primary reference is also withdrawn as the rejection appears to be accumulative.

*** Applicant's other remarks filed February 17, 2004 with respect to the claims have been considered but they are moot in view of the new ground(s) of rejection.

Forming the first electrode in a recess of the substrate assembly and extending above the uppermost surface of the substrate assembly, and forming the second electrode on the dielectric and on the uppermost surface of the substrate assembly are taught by the references including Agarwal and Chen, and would have been obvious to one of ordinary skill in the art so that the first electrode is formed in a recess opening of a substrate assembly contacting the underlying conductive layer for electrically connection. Moreover, Prall teaches fabricating a semiconductor device including a capacitor, wherein forming a first electrode in a recess of a substrate assembly including the insulating layer 36 and extending above the uppermost surface of the substrate assembly including insulating layer 36 are clearly shown at least in Figures 4-5, and would have been obvious to one of ordinary skill in the art so as to increase cell spacing of the capacitor.

Also, it would have been obvious to one of ordinary skill in the art to form the capacitor of Fukuzumi by employing the teaching of Chen to form the second electrode along and on the uppermost surface of the substrate assembly and laterally extend from the capacitor, because of the desirability to complete and facilitate the next level of electrical interconnections in forming an electrical contact to the second electrode 42 that is laterally extended from the first electrode, and formed on the uppermost surface of the substrate assembly including the insulating layer 32/28 (Chen, Fig 8; col 9, lines 55 through col 10, line 4).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-6

Michael Trinh
Primary Examiner